

SIMULATE PORTABLE APILL SETTINGS WITH PROTEUS TO INCREASE SYSTEM RELIABILITY AND MINIMIZE CONFIGURATION ERRORS

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ABSTRACT

APILL Portable is one of the traffic control systems that utilizes Arduino microcontroller technology to manage traffic lights, temperature sensors, and humidity. This system can be monitored in real-time, collecting traffic data that can be utilized to enhance traffic efficiency and safety. However, in its implementation, configuration errors often occur in APILL Portable settings, leading to system malfunction. Therefore, this research is conducted to optimize APILL Portable settings using Proteus with the aim of improving system reliability and minimizing configuration errors. In this study, an analysis of potential configuration errors in APILL Portable settings with Proteus will be performed through traffic simulation. Additionally, verification and validation methods will be developed to ensure that each configuration is precise and accurate.

Keywords: APILL; controlling system; proteus pro; simulation

INTRODUCTION

APILL Portable is a traffic management system that uses Arduino microcontroller technology to control traffic lights, temperature and humidity sensors. This system can be monitored in real-time and collect traffic data that can be used to improve traffic efficiency and safety. However, in its application, configuration errors often occur in the APILL Portable settings which result in the system not working properly so it is necessary to avoid cost overruns due to equipment damage caused by configuration errors. It is necessary to design the equipment through simulation, one of which is Proteus to save costs and make things easier if necessary. redeveloped (Adani, 2020). This is in line with research conducted by (Wendri, 2016) where it was obtained that Proteus simulation results could be used in sensor circuits using Arduino. Therefore, this research was conducted to optimize the APILL Portable settings with Proteus with the aim of increasing system reliability and minimizing configuration errors. In this research, an analysis of potential configuration errors will be carried out in setting up APILL Portable with Proteus in traffic simulations.

Next, this research will try to optimize the APILL Portable settings with Proteus by using available optimization techniques to minimize configuration errors and increase system reliability. In this research, we will also evaluate the performance of the APILL Portable system with Proteus in traffic simulations by considering various factors that influence system performance, such as system response, response time, energy use efficiency, and system reliability. It is hoped that the results of this research can contribute to the development and application of the Portable APILL system with Proteus which is more effective and efficient in managing road traffic. Apart from that, it is also hoped that this research can provide useful input in the development of more sophisticated and reliable microcontroller and traffic simulation technology in the future.

Research purposes The purpose of carrying out this research can be described as follows: To obtain a simulation model for a portable APILL system with Proteus To find out how to identify configuration errors in portable APILL systems with Proteus. To obtain comparison results of simulations with experimental data from the portable APILL that has been implemented

METHOD

Data sources are the main requirement in research. In this research, various data sources were obtained. To achieve the objectives of this research, the following data collection steps were carried out:

Research Location The case study that will be carried out in this research is located at the Bali Land Transportation Polytechnic Research Data This research uses two types of data consisting of primary data, namely data obtained from direct observations in the field, and secondary data, namely data obtained from literacy studies or previous research. Primary data collection uses direct observation in the field by observing the Proteus simulation process for compliance with APILL Portable based on the results of the field survey as follows:

Inventory data is obtained from the results of inventory surveys at road sections or study intersections. This data will be managed as a basis for calculating the capacity of the study road section. Traffic volume is obtained from the results of traffic enumeration surveys carried out on study road sections or turning movement surveys at intersections. This data will be managed into traffic performance on the study road section. Cycle time is the time allocated in the APILL program. This time is the result of management or final data that can be obtained from the results of calculating the performance of road sections and intersections. This cycle time can be displayed with a cycle time diagram. Secondary data is collected to support primary data collection and is used for the analysis process. Secondary data was obtained from previous research literacy studies. The research stages can be described in the flow chart in Figure 1 as follows.

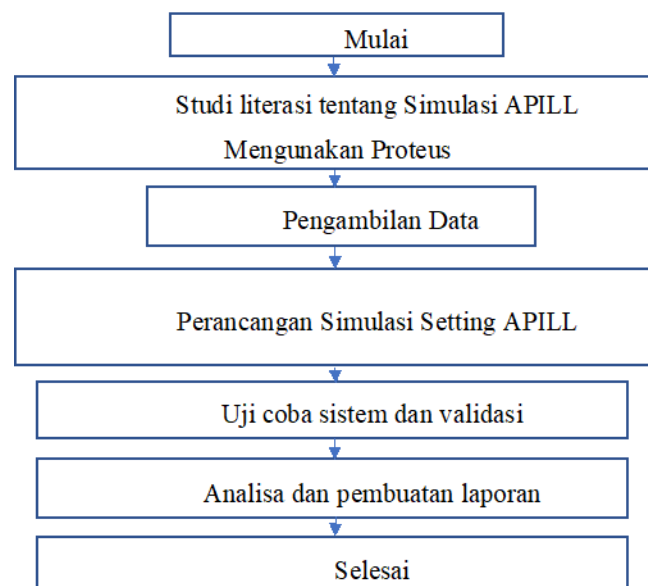


Figure 1 Flow Chart

The description of the activities that will be carried out in carrying out the research can be described as follows.

a. Literacy Studies

Literacy studies regarding the design of APILL Portable simulation settings using Proteus are the initial stage in carrying out this research. Literacy studies were carried out by searching for national and international journals, books, articles and research reports related to the APILL Portabel Controlling System and Proteus.

b. Data retrieval

Data collection is carried out by surveying traffic characteristics which will then be managed into the performance of roads and intersections to produce cycle times which will be outlined in a cycle time diagram.

c. APILL Setting Simulation System Design

The design of the APILL Portable setting simulation system uses the Proteus method by creating an Arduino control simulation.

d. System testing, analysis and validation. System testing is carried out by simulating the hardware installation design in the Proteus software to obtain an installation scheme that will later be created. The validation process will be carried out by seeing whether the hardware installation will run according to the simulation carried out in Proteus. This validation process looks at several parameters, namely whether an error occurred during installation and also whether the system (APILL time settings) runs according to the simulation. If the installation results are invalid or have an error, it is necessary to recalibrate by re-simulating the installation of the device in the Proteus application.

RESULTS AND DISCUSSION

Intersection Inventory Results

From the results of the inventory survey at the Dalung LPD Intersection, it was found that the existing geometric conditions influenced the determination of cycle times. The Dalung LPD intersection is intersection 4 with APILL settings but is not operational so the existing APILL is only used as flashing or only the yellow/amber lights are on. At the foot of the intersection there is no median and the surrounding land use is shops. Side obstacles are generally moderate, here is a visual of the LPD Dalung intersection in the form of photos and layout of the intersection as a result of the inventory survey.

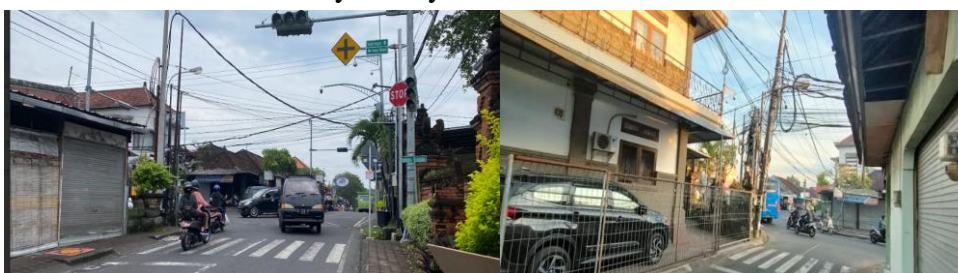


Figure 2 Visual of the LPD Dalung intersection Figure 2 Visual of the LPD Dalung intersection

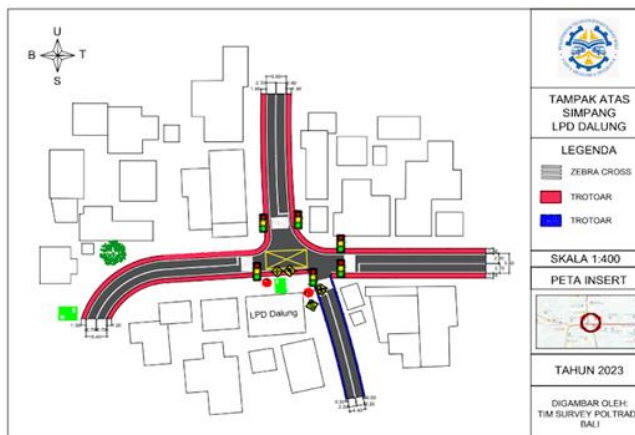


Figure 3 Layout of the Dalung LPD intersection

Traffic Volume Data

From the results of the survey on the volume of turning movements carried out during busy times, the volume of turning movements from each leg of the intersection was obtained. The volume that has been obtained is then poured into the intersection flow diagram as seen in Figure 4 below:

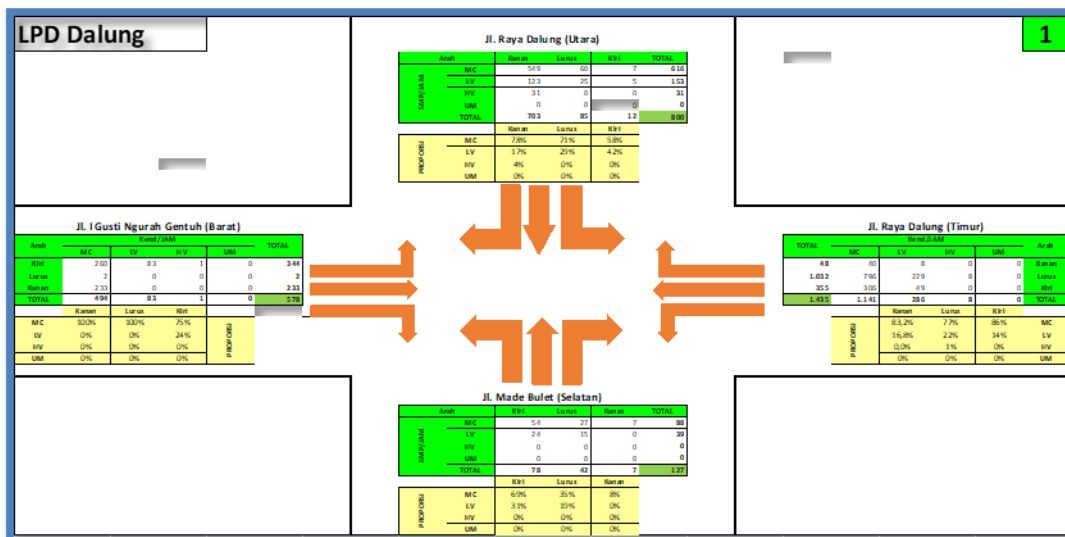


Figure 4. Flow diagram of the Dalung LPD intersection

The flow diagram in Figure 4 is one of the determining factors for the flow ratio on each arm, where this is a step to obtain cycle times that are appropriate to traffic conditions.

Cycle Time Calculation

One of the most important components in making the APILL Portable electronic design is input data in the form of cycle time which consists of green time, yellow time and Allred time. The data previously submitted is the data needed to calculate cycle time according to the PKJI 2023 method. The following are the stages in determining cycle time:

1. Determination of saturation current for each approach

At the Dalung LPD intersection, it is planned to use a 4-phase arrangement, this is because the right-turning current is high compared to the countercurrent or straight-line current from the opposite arm. So the basic saturation current is determined by calculating the effective approach width of 600. The basic saturation current will then be multiplied by a correction factor

according to the geometric conditions and side obstacles resulting from the inventory survey. The following are the results of the saturation current for each approach.

Table 1.
 Table for Determination of Saturated Current

Kaki Simpang	Approach	We	Jo	Fuk	Fg	Fp	Arus Jenuh
Jl. Raya Dalung	North	4,5	2.700	0,94	1	1	2.538
Jl. Made Bulet	South	2,5	1.500	0,94	1	1	1.410
Jl. Raya Dalung	East	4,5	2.700	0,94	1	1	2.538
Jl. Gst. Nrh. Gentuh	West	4	2.400	0,94	1	1	2.256

2. Determination of the Deviation Flow Ratio (IFR)

Intersection flow ratio (IFR) is a calculation of the ratio between current (Q) and saturation current (J) so that the current ratio (FR) is obtained for each approach and then the highest or critical FR (Frcrit) of the approach is selected. who are in the same phase. In calculating the Dalung LPD Intersection, it is planned to use 4 phases so that all FRs are considered critical so that to obtain the IFR you need to add up all the FRs for each approach at the Dalung LDP intersection. The following are the results of the IFR calculation for the LPD Dalung intersection.

Table 2.
 IFR Calculation Results at the Dalung LPD Intersection

Kaki Simpang	Approach	Arus (Q)	Arus Jenuh	FR	IFR
Jl. Raya Dalung	North	800	2.538	0,32	0,95
Jl. Made Bulet	South	127	1.410	0,09	
Jl. Raya Dalung	East	765	2.538	0,30	
Jl. Gst. Nrh. Gentuh	West	543	2.256	0,24	

3. Determination of Cycle Time

From the results of previous IFR calculations, temporary cycle time was determined as a component to find the green time distribution for each phase or intersection leg. To determine the time between greens (amber and allred) use standard settings, namely amber 3 seconds and allred 2 seconds so that the time between greens for each phase is 5 seconds. From determining the time between greens, the total for the number of phases is then added and the total lost time intersection (LTI) is 20 seconds. The following is a table of the Dalung LPD intersection cycle time calculation results.

Table 3.
 Cycle Calculation Results

Kaki Simpang	Approach	Siklus Pra Penyesuaian	Waktu Hijau	WHH	Siklus
Jl. Raya Dalung	North	237,60	77,39	5	252,60
Jl. Made Bulet	South		22,11	5	
Jl. Raya Dalung	East		74,00	5	
Jl. Gst. Nrh. Gentuh	West		59,09	5	

The result obtained was 252.60 seconds, which is in accordance with the instructions in the PKJI to avoid cycle times of more than 130 seconds except for intersections that have large geometric shapes. Looking at the geometric conditions of the Dalung LPD intersection, a decision was made to use the maximum feasible green time for the 4 phases in accordance with the instructions from PKJI 2023. The following is the distribution of green time using the appropriate cycle time.

Table 4.
 Adjustment Cycle Time

Kaki Simpang	Approach	Siklus Pra Penyesuaian	Waktu Hijau	WHH	Siklus
Jl. Raya Dalung	North	130	36	5	130
Jl. Made Bulet	South		11	5	
Jl. Raya Dalung	East		35	5	
Jl. Gst. Nrh. Gentuh	West		28	5	

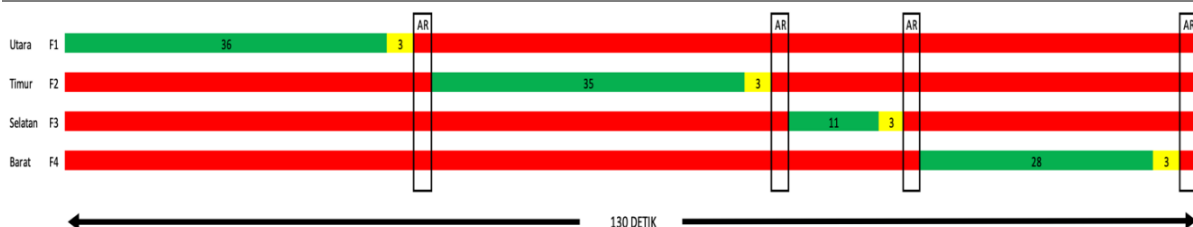


Figure 5 Dalung LPD Intersection Cycle Time Diagram

Complete Design and Simulation of Proteus

In creating a complete design and Proteus simulation there are several stages until the results can be applied in real terms. The following are the stages in making the model:

1. Making a complete design for APILL Portable

From the master and slave design, the overall electronic system design can be determined for making a complete Portable APILL which consists of 4 APILL poles. The following is the overall system design as seen in Figure 6

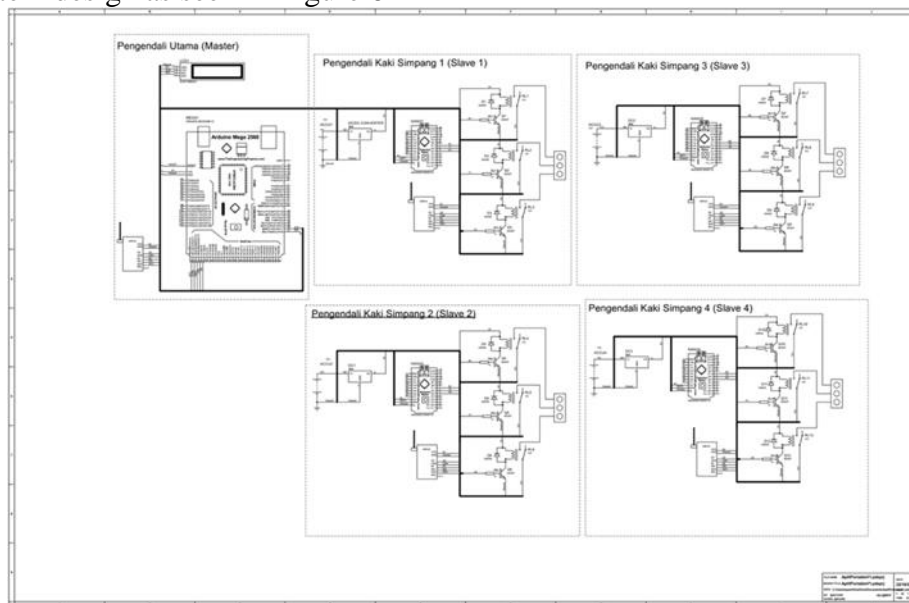


Figure 6 Overall APILL Electronic Circuit Design

2. Design Simulation Using Proteus

The next stage is to simulate whether the APILL Portable electronic design prototype that has been designed can be implemented using the help of the Proteus application. This application is very helpful in reducing the risk of damage and failure due to errors in component installation or errors in the electronic design that has been made. This is done to ensure that the design that has been created can later be implemented in reality. The following visual appearance is sampled at only one leg of the intersection (Intersection leg 1) including green, amber, allred, red.

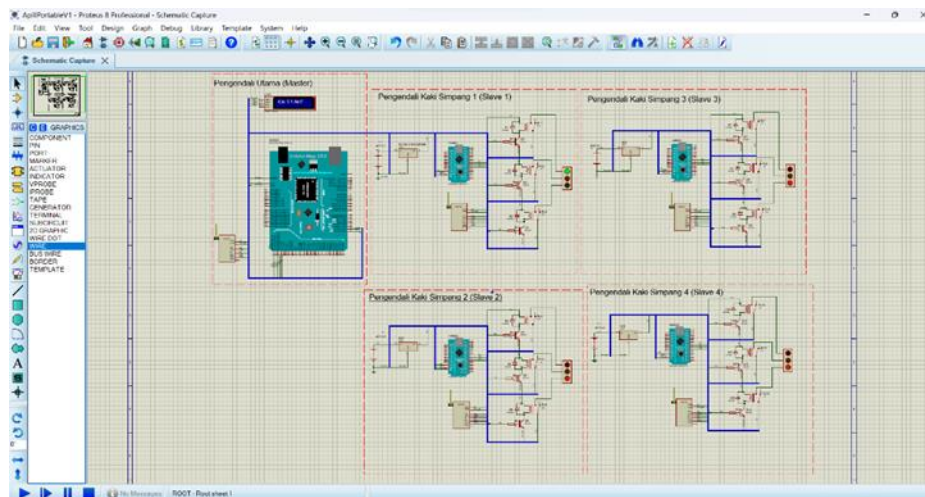


Figure 7 Visual appearance of time at intersection leg 1

3. Design Simulation Data Results

From the results of the first simulation, Proteus simulation log data is produced, where simulation log data refers to notes or recordings of simulation results data that can be saved for further analysis. This simulation log data is used in understanding circuit performance and analyzing its response to certain conditions. The following is the simulation log data which can be seen in Figure 8.

Proteus Simulation Running Summary 22/10/2023 ; 19:28:13Z	
VOLTAGE (volt)	
* Moga 2650	= 5.2v
* Nano_1	= 5.2v
* Nano_2	= 5.2v
* Nano_3	= 5.2v
* Nano_4	= 5.2v
* nRF24L01_1_TX	= 5.3v
* nRF24L01_2_RX	= 5.3v
* nRF24L01_3_RX	= 5.3v
* nRF24L01_4_RX	= 5.3v
* nRF24L01_5_RX	= 5.3v
* Relay Module_1	supply = 5.1v ; NO Out = 12.79v
* Relay Module_2	supply = 5.1v ; NO Out = 12.79v
* Relay Module_3	supply = 5.1v ; NO Out = 12.79v
* Relay Module_4	supply = 5.1v ; NO Out = 12.79v
* Aspect Light_1	= 12.79v
* Aspect Light_2	= 12.79v
* Aspect Light_3	= 12.79v
* Aspect Light_4	= 12.79v
* Accu_1	= 12.79v
* Accu_2	= 12.79v
* Accu_3	= 12.79v
* Accu_4	= 12.79v
* DC/DC Converter_1	Vin = 12.78v ; Vout = 5.4v
* DC/DC Converter_1	Vin = 12.78v ; Vout = 5.4v
* DC/DC Converter_1	Vin = 12.78v ; Vout = 5.4v
* DC/DC Converter_1	Vin = 12.78v ; Vout = 5.4v
Time Domain (millisecond)	
* nRF24L01_TX	= 0ms
* nRF24L01_RX	= 3470ms
* GreetLine-1	= 12000ms
* GreetLine-2	= 12000ms
* GreetLine-3	= 12000ms
* GreetLine-4	= 12000ms

Figure 8 Initial design simulation log data

Through simulation data it can be seen:

- The voltage obtained on each component is at the normal figure of 12.79 volts maximum and 5.4 volts maximum and is still within the recommended tolerance limit except for the nRF24101 module which obtains a voltage of 4.3 volts from the 5V requirement.
- There was a delay in sending the data signal from the Master (nRF24101_TX) to the Slave (nRF24101_RX) of 3.47 seconds, so there was a delay in the expected cycle time.

4. Circuit Correction

Based on the simulation results listed in the summary log, corrections need to be made to the circuit by adding a buffer component in the form of an IN4733A/5.1V Zener diode to the DC-DC converter to obtain sufficient voltage on the nRF24101 module.

5. Simulation Log Data Correction Results

The following are the results of the correction design simulation output log:

Proteus Simulation Running Summary 22/10/2023 ; 23:49:145	
VOLTAGE (volt)	
* Mega 2650	= 5.1v
* Nano_1	= 5.1v
* Nano_2	= 5.1v
* Nano_3	= 5.1v
* Nano_4	= 5.1v
* nRF24L01_1_TX	= 5.1v
* nRF24L01_2_RX	= 5.1v
* nRF24L01_3_RX	= 5.1v
* nRF24L01_4_RX	= 5.1v
* nRF24L01_5_RX	= 5.1v
* Relay Module_1	supply = 5.1v ; NO But = 12.79v
* Relay Module_2	supply = 5.1v ; NO But = 12.79v
* Relay Module_3	supply = 5.1v ; NO But = 12.79v
* Relay Module_4	supply = 5.1v ; NO But = 12.79v
* Aspect Light_1	= 12.79v
* Aspect Light_2	= 12.79v
* Aspect Light_3	= 12.79v
* Aspect Light_4	= 12.79v
* Accu_1	= 12.79v
* Accu_2	= 12.79v
* Accu_3	= 12.79v
* Accu_4	= 12.79v
* DC/DC Converter_1	Vin = 12.78v ; Vout = 5.1v
* DC/DC Converter_1	Vin = 12.78v ; Vout = 5.1v
* DC/DC Converter_1	Vin = 12.78v ; Vout = 5.1v
* DC/DC Converter_1	Vin = 12.78v ; Vout = 5.1v
Time Domain (millisecond)	
* nRF24L01_TX	= 0ms
* nRF24L01_RX	= 0.828ms
* Greetime-1	= 12000ms
* Greetime-2	= 12000ms
* Greetime-3	= 12000ms
* Greetime-4	= 12000ms

Figure 9 Correction design simulation log data

Through simulation data it can be seen:

- The voltage obtained on each component is at the normal figure of 12.79 volts maximum and 5.1 volts maximum and is still within the recommended tolerance limits.
- There was an improvement in the voltage value on the nRF24101 module from 4.3volts to 5.1volts so that the power requirements for this component were met.
- The time for sending data signals from the Master (nRF24101_TX) to the Slave (nRF24101_RX) is better and only takes a very short time and is instantaneous with a duration of 28us or 0.028 seconds. This is due to the stability of the voltage on the nRF24101 radio transmitter and receiver modules.

6. Results of Electronic Design Installation

The complete electronic design or wiring diagram that has been successful in the appropriate Proteus simulation is then used as a reference in installing the electronic system components of the Portable APILL on each of the intersection foot posts. The installation results can be seen in Figure 10 below.

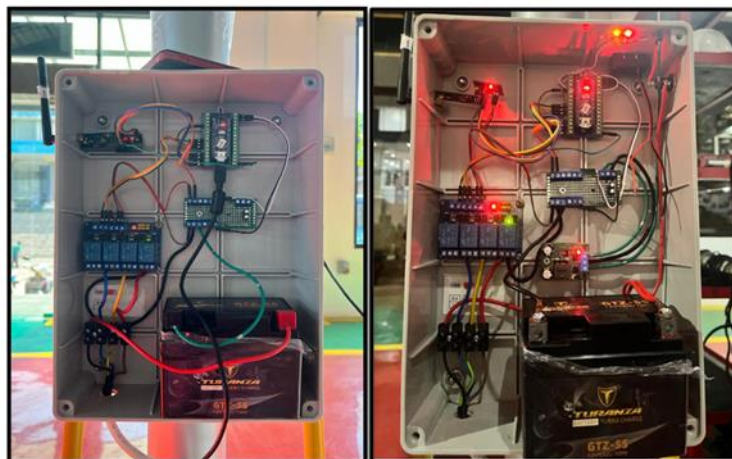


Figure 10 Results of installing electronic components

7. Test Time Display

After the electronic device can work without errors, a test is carried out to match the display time with the previously set time. The test is carried out by calculating the time manually using a stopwatch by paying attention to the length of time the aspect lamp lights up. The time tested is the green time that appears on the side lights of each portable APILL pole. The following are the results of the resulting time comparison.

Table 5.
 Device Green Time Test Results

Fase Tiang	Comparison	Waktu Hijau siklus 1	Waktu Hijau siklus 2	Waktu Hijau siklus 3	Waktu Hijau siklus 4	Waktu Hijau siklus 5
F1	Count	36	36	36	36	36
	Test	36,20	36,07	36,00	36,17	36,12
F2	Count	35	35	35	35	35
	Test	35	35,4	35,03	35,23	35,16
F3	Count	11	11	11	11	11
	Test	11,21	11,14	11,09	11,05	11,2
F4	Count	28	28	28	28	28
	Test	28,17	28,2	28,26	28,08	28,14

From the test results it can be seen that there is a slight time deviation between the time set and the time calculated using a stopwatch. This is due to the response factor of the officers who calculate the time. However, if we look at Table 6.1, it can be stated that the designed APILL Portable electronic system can function well and produce aspect lengths that are in accordance with the calculations.

CONCLUSION

In carrying out the research stages, the research team can draw several conclusions from the results obtained. These conclusions can be described as follows: The APILL Portable electronic system design has been produced with simulation results using Proteus stating that the system can work well. There are several risks of error, such as a delay in sending the data signal from the Master (nRF24I01_TX) to the Slave (nRF24I01_RX) of 3.47 seconds, resulting in a delay in the expected cycle time. Cycle time from the green count time test results with the visual green time of the APILL Portable aspect light. It can be concluded that the APILL Portable cycle time is in accordance with the count time so that the electronic system design simulated in Proteus can be used properly.

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